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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/699,947	10/30/2000	Edmund J. Kelly	TRANS04D	8830

7590 11/17/2004

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EXAMINER	
THAI, TUAN V	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/699,947	KELLY ET AL.	
	Examiner	Art Unit	
	Tuan V. Thai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3, 5-9, 12-13 and 18-20* is/are pending in the application.

4a) Of the above claim(s) *4,10,11 and 14-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-9,12,13 and 18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/29/04; 09/15/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. This office action responsive to a request for continued examination under 37 CFR 1.114. Applicant's submission filed on March 29, 2004 has been entered. Claims 1-3, 5-9, 12-13 and 18-20 are presented for examination. Claims 4, 10-11 and 14-17 have been cancelled.

2. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.

Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 5-9, 12-13 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moore et al. (USPN: 5,437,017), hereinafter Moore, in view of IBM TDB, May 1994, Vol. 37, Issue 5, pages 249-250; hereinafter IBMTDB 37.

As per claim 1, Moore teaches the invention as claimed including a method and system for protecting memory from being written in a computer [6] which includes a host processor [10] designed to execute instructions of a host instruction set and software synchronization utilized for instruction/data translation and TLB coherency (e.g. see column 2, lines 36-37) comprises hardware means having a translation lookaside buffer with a storage position in each storage location included in each processor for translating an effective or virtual address to a real address within system memory (e.g. see figure 1; column 4, lines 19 et seq.); software means responding to an indication ... once the memory address has been written is taught as the software implementation of a translation lookaside buffer invalidate (TLBI) instruction or by software synchronization throughout the multiprocessor data processing system (e.g. see column 2, lines 36-37; figure 5, column 8, lines 32 et seq.). Moore discloses the invention as claimed except for means for indicating whether memory address stores target instruction which has been translated into host instruction. IBMTDB 37, in its teaching of the use of the SYNC instruction to synchronize completion of Translation Lookaside Buffer Invalidate in Multiprocessor system, discloses the means for indicating whether memory address stores target instruction which has been translated into host instruction as being equivalent to the SYNC operation instruction signal received from the receiving

processor after broadcasting of the TBLI instruction for indicating of whether the instruction has been translated/ executed within the local receiving processor (TBLI instruction has taken effect throughout the SMP environment; e.g. see disclosure text). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to utilize the means for indicating whether memory address stores target instruction which has been executed/translated into host instruction (being equivalent to the SYNC operation signal) as taught and being disclosed in the IBM TDB 37 for that of Moore's system in order to arrive at Applicant's current invention. In doing so, it would enhance system reliability and throughput by allowing the host in Moore's system to quickly and uniformly execute instructions wherein only instructions which has been translated from target into host instruction can be executed, therefore being advantageous.

As per claim 2, Moore further discloses the memory management unit 34 (hardware means) comprises look-aside buffer 40 having plurality of storage locations for virtual addresses and associated physical addresses, and a storage position in each storage location (e.g. see figure 3; column 6, lines 22 et seq.);

As per claim 3, software means for invalidating host instruction translated from target instructions stored at the memory address is clearly taught by Moore as the software synchronization throughout the multiprocessor data processing

system, also by the software implementation of a translation lookaside buffer invalidate (TLBI) (e.g. see column 2, lines 36-37; figure 5, column 8, lines 32 et seq; also see abstract, column 3, lines 12 et seq.);

As per claim 5, Moore discloses software means for protecting against writing the memory address removes translations associated with the memory address is taught as software synchronization and means for purging all instructions within the plurality of processors for achieving coherency (e.g. see column 2, lines 36-37; and claims 12 and 13);

As per claim 6, Moore further discloses the memory management unit 34 (hardware means) comprises look-aside buffer 40 having plurality of storage locations for virtual addresses and associated physical addresses, and a storage position in each storage location (e.g. see figure 3; column 6, lines 22 et seq.); software means for protecting against writing the memory address removes translations associated with the memory address is taught as software synchronization and means for purging all instructions within the plurality of processors for achieving coherency (e.g. see column 2, lines 36-37; and claims 12 and 13);

As per claims 7 and 8, see arguments with respect to claim 1; in addition, Moore further discloses hardware means for generating and exception to a write access ... to a host instruction as being equivalently taught as means for suspending execution of instructions within each of said plurality of

processors until coherency is achieved (e.g. see claim 12); Moore also discloses the memory management unit 34 (hardware means) comprises look-aside buffer 40 having plurality of storage locations for virtual addresses and associated physical addresses, (e.g. see figure 1; column 2, lines 7 et seq.; figure 3; column 6, lines 22 et seq.);

As per claim 9, software means responding to an exception to a write ... will not be utilized before being updated is taught as software synchronization and means for purging all instructions within the plurality of processors for achieving coherency (e.g. see column 2, lines 36-37; and claims 12 and 13); also the processing of a translation lookaside buffer invalidate (TLBI) instruction throughout the multiprocessor data processing system (e.g. see figure 5, column 8, lines 32 et seq.);

As per claims 12 and 13, they encompass the same scope of invention as to that of claim 1, except that they are drafted as method format rather apparatus format, the claims are therefore rejected for the same reasons as being set forth above.

As per claims 18-20, they encompass the same scope of invention as to that of claims 1-3, it should further be noted that the memory controller being claimed in claim 18 in which it comprises a translation lookaside buffer... etc, is equivalent to the memory management unit (MMU) having a TLB (e.g. see figure 3), and other equivalent elements as detailed in claims 1-3. The claims therefore are rejected for the same reason as set forth

above. It should be noted that the concept of target instruction being translated into host instruction wherein code intended for a first target processor is translated into code for running on different host processor which is clearly taught by Moore starting on column 4, lines 19 et seq.; for example, Moore does disclose that if the conditional branch is predicted as "taken" then the target instruction is utilized, otherwise it is purged, and the sequential instruction is retrieved.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

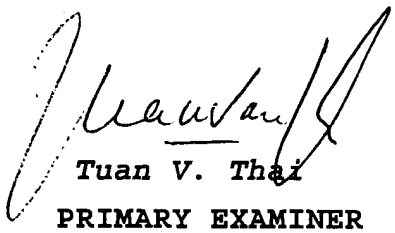
6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-4187. The examiner can normally be reached on from 6:30 A.M. to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (571)-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be

obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see ***http://pair-direct.uspto.gov***. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/November 10, 2004



Tuan V. Thai
PRIMARY EXAMINER
Group 2100